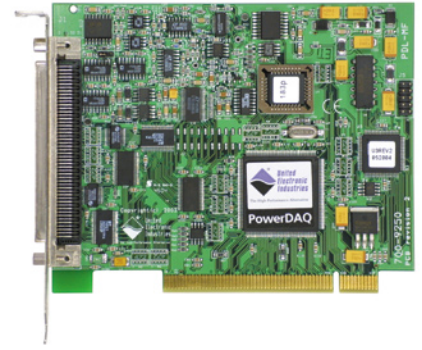


# PDL-MF

## PowerDAQ Lab PCI Multifunction Board

- 16 single-ended/16 pseudo-differential or 8 differential A/D channels
- 16-bit, 50 kS/s sampling rate
- Two 12-bit analog outputs; 48 digital I/O lines; three 24-bit counter/timers
- Simultaneous operation of all subsystems
- 64 entries in channel-gain list; programmable gains: 1, 2, 5, 10
- Stream-to-disk capability



Supports **UEIDAQ Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

### General Description:

The data-acquisition community has come to appreciate the power and flexibility of the architecture in the PowerDAQ II family of PCI data acquisition cards. They've also come to value the easy programming this architecture affords as well as the extensive support software that accompanies each board. Now UEI is making it even easier for users to take advantage of these features by lowering the entry-level price. This comes with the most recent member of the PCI-bus PowerDAQ family: the PowerDAQ Lab card.

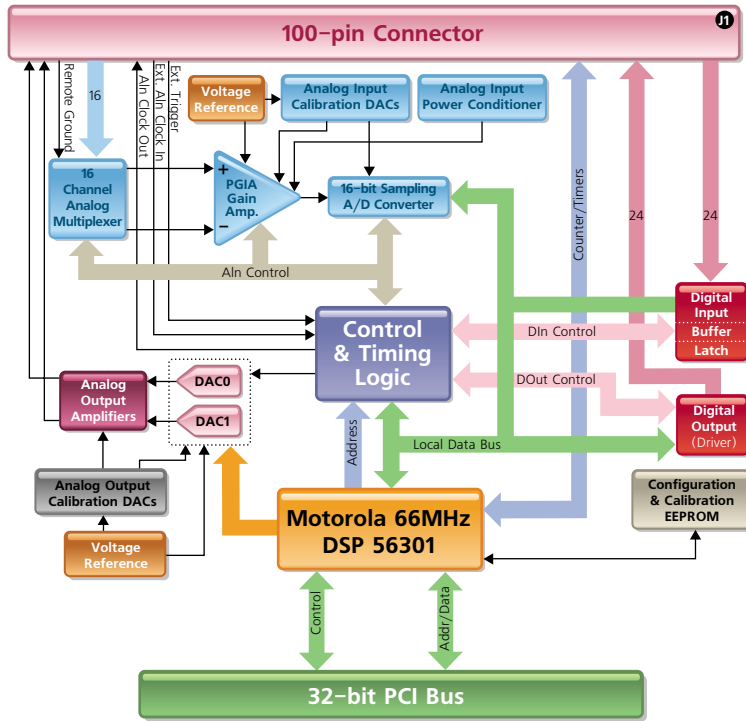
Not only does this latest member drop the price considerably over the previous member with similar functionality, it does so in a short-slot card, making it suited for positioning in chassis slots shortened by peripherals or in laptop PCs with limited slot sizes. Nonetheless, it does not sacrifice on any of the functionality users have come to expect in a PowerDAQ card, because this multifunction card supplies a full complement of analog I/O as well as digital I/O - and all these subsystems can run simultaneously.

### Technical Specifications:

Analog Inputs	
Resolution	16 bit
Number of channels:	
Single-Ended	16
Pseudo-Differential	16
Differential	8
Max. sampling rate	50 kS/s
Onboard FIFO	1k samples
Channel gain list	64 entries
Input ranges	0-10V, $\pm 5V$ , $\pm 10V$ (softw. selectable)
Max working voltage for Ain	
single-ended	$\pm 10V$
differential	$\pm 13V$ (signal + common mode)
pseudo-differential	$\pm 13V$ (signal + EXT_GND)
Programmable gains	1, 2, 5, 10
Drift	
Zero	$\pm 30 \mu V/^{\circ}C$
Gain	$\pm 30 \text{ ppm}/^{\circ}C$
Input impedance	10M $\Omega$
Input bias current	$\pm 20 \text{ nA}$
Input Overvoltage	$\pm 35V \text{ cont.}, 10mA \text{ max}$
A/D conversion time	2 $\mu s$
A/D settling time	4.1 $\mu s$ (@ g=1)
DC Accuracy	
Nonlinearity	$\pm 1 \text{ LSB}$
System noise	1.2 LSB
AC Accuracy	
Effective number of bits	14.8
Channel crosstalk	-80 dB @ 1kS/s
Clocking and Trigger Input	
Max. A/D pacer clock aggregate throughput @ 0.01% accuracy	50 kS/s
External A/D sample clock maximum frequency	50 kHz
Minimum pulse width	20 ns
External digital (TTL) trigger:	
High-level input voltage	2.0V min
Low-level input voltage	0.8V min
Minimum pulse width	20 ns
Digital trigger	start/stop

Analog Outputs	
Number of channels	2
Resolution	12 bits
Update rate	100 kS/s each
Onboard FIFO	2k samples; 64k samples with PD-64KMEM upgrade option
Analog output range	$\pm 10V$
Current output	$\pm 20 \text{ mA max}$
Output impedance	0.3 $\Omega$ typ
Capacitive drive capability	1000 pF
Nonlinearity	$\pm 1 \text{ LSB}$
Protection	short circuit to analog ground
Power-on voltage	0V $\pm 10 \text{ mV}$
Settling time to 0.01% of FSR	10 $\mu s$ , 20V step; 1 $\mu s$ , 100mV step
Slew rate	30 V/ $\mu s$
Digital I/O	
Input channels	24
Output channels	24
High-level input voltage	2.0V min
Low-level input voltage	0.8V max
High-level input current	20 $\mu A$
Low-level input current	-20 $\mu A$
Output driver high voltage	2.5V min, 3.0V typ ( $I_{OH} = -32mA$ )
Output driver low voltage	0.55V max ( $I_{OL} = 64mA$ )
Current sink	-32/64 mA max, lines 8-16 -24/24 mA max, lines 0-7 250mA per port
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock, 33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock, no low limit for external clock
Min pulse width	20 ns
Output high level	2.0V min @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, $\pm 30V$ over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

## Block Diagram:

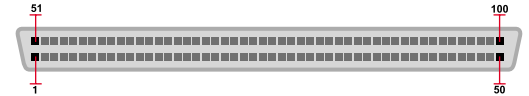
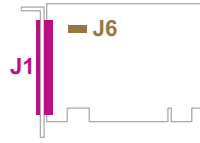


## Pinout Diagrams:

J1 – 100-pin connector (female):

AIN8	1	51	AIN0
AGND	2	52	AGND
AIN9	3	53	AIN1
AGND	4	54	AGND
AIN10	5	55	AIN2
AGND	6	56	AGND
AIN11	7	57	AIN3
AGND	8	58	AGND
AIN12	9	59	AIN4
AGND	10	60	AGND
AIN13	11	61	AIN5
AGND	12	62	AGND
AIN14	13	63	AIN6
AGND	14	64	AGND
AIN15	15	65	AIN7
AGND	16	66	EXT_GND
AOUT0	17	67	AOUT1
AGND	18	68	AGND
DIN1	19	69	DIN0
DIN3	20	70	DIN2
DIN5	21	71	DIN4
DIN7	22	72	DIN6
DIN9	23	73	DIN8
DIN11	24	74	DIN10
DIN13	25	75	DIN12
DIN15	26	76	DIN14
DIN17	27	77	DIN16
DIN19	28	78	DIN18
DIN21	29	79	DIN20
DIN23	30	80	DIN22
DIN25	31	81	DIN24
DOUT1	32	82	DOUT0
DOUT3	33	83	DOUT2
DOUT5	34	84	DOUT4
DOUT7	35	85	DOUT6
DGND	36	86	+5VRI2
DOUT9	37	87	DOUT8
DOUT11	38	88	DOUT10
DOUT13	39	89	DOUT12
DOUT15	40	90	DOUT14
DOUT17	41	91	DOUT16
DOUT19	42	92	DOUT18
DOUT21	43	93	DOUT20
DOUT23	44	94	DOUT22
DGND	45	95	DGND
EXT_TRIG_IN	46	96	TMR2
CV_OUT	47	97	DGND
EXT_TRIG_OUT	48	98	TMR1
CL_OUT	49	99	DGND
EXT_CLK	50	100	TMR0

J6 – 3-pin jumper header:



## Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J1	PDL-CBL-100*	PDL-STP	Carries 16 analog input lines, 2 analog output lines, 24 digital input and 24 digital output lines, 3 counter/timer lines to terminal panel. PDL-STP allows further connection to 5B signal conditioning panel (for analog input signals).

\* Pins 1 - 50 from PDL-MF's J1 connector are transferred to the first 50-pin IDC header of PDL-CBL-100 cable without remapping (pin-to-pin number match). Remaining 51 - 100 pins are transferred to the second 50-pin IDC header as follows: 51 to 1, 52 to 2, ... 99 to 49, 100 to 50.

## Analog Input Configuration:

Configuration is performed using J6 jumpers.

J6 Jumper Position	Analog Input Configuration						
<table border="1"> <tr><td>3</td><td>2</td><td>1</td></tr> <tr><td>○</td><td>○</td><td>○</td></tr> </table>	3	2	1	○	○	○	pseudo-differential
3	2	1					
○	○	○					
<table border="1"> <tr><td>3</td><td>2</td><td>1</td></tr> <tr><td>○</td><td>○</td><td>○</td></tr> </table> (default)	3	2	1	○	○	○	single-ended differential
3	2	1					
○	○	○					