

PDXI-AO-8/16

8-Channel cPCI/PXI Card for Analog Output Data Acquisition

- 8 analog outputs (16-bit resolution)
- 8 digital inputs; 8 digital outputs
- Three 24-bit counters/timers
- Three clock/interrupt lines
- Channel list (64 locations)
- Independent waveform on each channel
- Simultaneous channel update; update on external event
- 2k samples onboard buffer size (upgradable to 64K samples)



Supports **UEIDAQ Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description:

A member of UEI's PDXI family of CompactPCI-compatible cards, the PDXI-AO-8/16 supplies as many as 8 independent 16-bit analog outputs on a C-sized card. Here you not only significantly increase the number of analog outputs, you also have 16 digital I/O lines and three counter/timers. With these functions, the PDXI-AO is well suited to implement complex closed-loop systems as well as handle motor control and many other industrial-automation tasks.

The card calibrates each analog output individually without using trim pots. Instead relies on a special D/A-based scheme that stores calibration coefficients in EEPROM and loads them automatically upon power up. This method also keeps board outputs in a predefined user-programmable state upon system startup.

Technical Specifications:

Analog Outputs	
Number of channels	8
Resolution	16 bits
Update rate	100 kS/s per channel; 450kS/s aggregate in non-DMA mode; up to 800 kS/s aggregate in DMA mode
DSP buffer size	2k samples (2 buffers x 1k sample)
Type of D/A	double-buffered
Data transfer modes	DMA, interrupt, software
Accuracy	±3 LSB max
DNL	±3 LSB max
Monotonicity over temp.	15 bits, -40 to 85°C
Calibrated gain error	3mV typ, 6mV max @ ±9.8V
Calibrated offset error	2mV typ, 3mV max @ 0.0V
Output range	±10V (custom ranges available)
Output coupling	DC
Output impedance	0.15Ω max
Current drive	±5 mA min
Capacitive loads	180 pF min
Settling time	10μs to 0.003%
Slew rate	10V/μs
Gain bandwidth	1 MHz
Noise	2 LSB RMS, 0-10000 Hz
Output protection	short to ground, ±15V
Power-on state	0.0000V ±5mV (default), user programmable
Gain drift	25 ppm/°C

Digital I/O	
Number of channels	8 inputs, 8 outputs
Compatibility	CMOS/TTL, 2kV ESD protected
Power-on state	logic zero (default), user programmable
Data transfer modes	DMA, interrupt, software
Input termination	4.7kΩ pull-up to 5V
Output high level	3.0V typ @ -32mA, 3.4V typ @ -16mA, 4.2V @ -2mA
Output low level	0.55V max @ 64mA
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock, 33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock, no low limit for external clock
Min pulse width	20 ns
Output high level	2.9V typ @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, ±30V over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

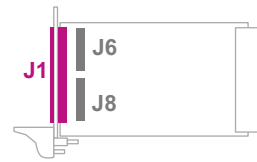
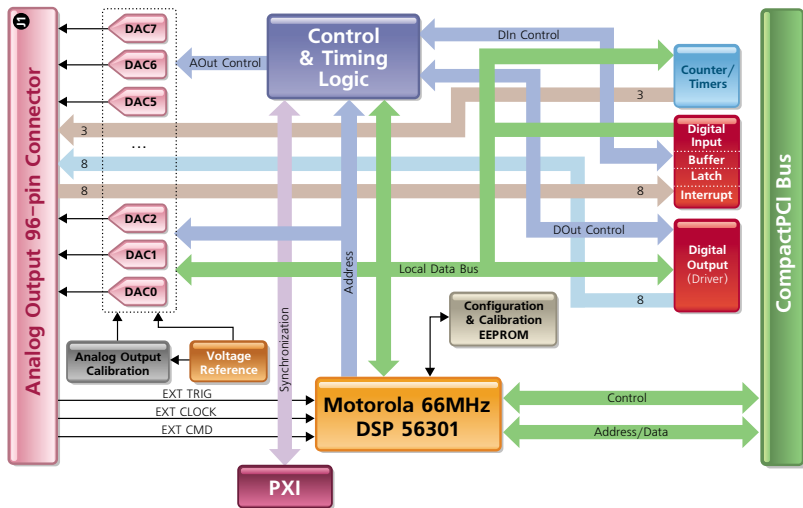
Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J1	PDXI-AO-CBL-96*	PD2-AO-STP-16	Carries 8 analog output, 8 digital input and 8 digital output lines to 16-channel terminal panel
J1	PDXI-AO-CBL-96	PD-AO-AMP-100	Carries 8 analog output lines to ±100V amplifier
		PD-STP-3716	Carries 16 digital I/O lines to 16-channel terminal panel
J1	PDXI-AO-CBL-96	PD-AO-AMP-115	Carries 8 analog output lines to ±115V amplifier
		PD-STP-3716	Carries 16 digital I/O lines to 16-channel terminal panel
J1	PDXI-AO-CBL-96	PD-BNC-16**	Carries 8 analog output, 8 digital input and 8 digital output lines to 16-channel terminal panel

* PDXI-AO-CBL-96 is a Y-split cable. Refer to the last page of this document for PDXI-AO-CBL-96 pinout diagram.

** PD-BNC-16 was initially designed for analog input subsystem of UEI's multifunction boards. Thus the analog output signals transferred via PDXI-AO-CBL-96 will not match the signal designations on PD-BNC-16's J1 connector. See PowerDAQ Analog Output Manual for more details and remapping diagram.

Block Diagram:



J6 — 4 x 16 jumper header:

AOUT3	43	21
AOUT2	42	20
AOUT1	41	19
AOUT0	40	18
AOUT7	39	17
AOUT6	38	16
AOUT5	37	15
AOUT4	36	14
AOUT11	35	13
AOUT10	34	12
AOUT9	33	11
AOUT8	32	10
AOUT15	31	9
AOUT14	30	8
AOUT13	29	7
AOUT12	28	6

J8 — 2 x 16 jumper header:

AOUT16	21
AOUT17	20
AOUT18	19
AOUT19	18
AOUT20	17
AOUT21	16
AOUT22	15
AOUT23	14
AOUT24	13
AOUT25	12
AOUT26	11
AOUT27	10
AOUT28	9
AOUT29	8
AOUT30	7
AOUT31	6

Sensing Configuration:

Remote sensing is available for the channels 0 - 7 only. Channels 8 - 15 are not available; J6 jumpers I - P should be installed in 3-4 position only - this will connect AOUT(8-15) SENSE lines to the ground and keep AOUT(8-15) lines not connected. Channels 16 - 31 are not available and corresponding lines in PDXI-AO-CBL-96 should be grounded using J8 jumper set (all jumpers should be populated in 1-2 position).

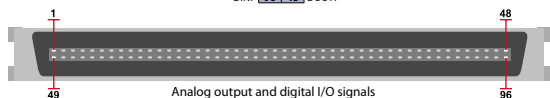
		PDXI-AO-8/16 (channels 0 - 7)		PD2-AO-STP-16	
		Jumper Position (A - P) ¹	Signals	Jumper Position (JP1 - JP16) ³	Signals
Sensing	Local	4 3 2 1 	AOUTX ² carries actual analog output signals and AOUTX SENSE ² carries analog ground. No compensation for the voltage drop across the cable (PDXI-AO-CBL-96).	A B C D 	OUTX ³ carries actual analog output signal; SNSX ³ is not connected
	Remote on STP	4 3 2 1 	AOUTX SENSE ² line is used to sense and compensate for the voltage drop across the cable (PDXI-AO-CBL-96). Voltage drop across the load wiring is not compensated.	A B C D 	OUTX ³ carries actual analog output signal; SNSX ³ carries analog ground
	Remote at load	4 3 2 1 	AOUTX SENSE ² line is used to sense and compensate for the voltage drop across the cable (PDXI-AO-CBL-96). Voltage drop across the load wiring is compensated.	A B C D 	OUTX ³ carries actual analog output signal; SNSX ³ carries actual analog output sense signal; OUTX ³ and SNSX ³ should be tied together at the load

¹ As designated on the PDXI-AO-8/16 board; ² As designated in pinout diagram for the J1 connector (PDXI-AO-8/16); ³ As designated on the PD2-AO-STP-16 terminal panel

Pinout Diagram:

J1 — pinless SCSI (male) 96-pin connector:

AOUT3	49	1	AOUT3 SENSE
AOUT2	50	2	AOUT2 SENSE
AOUT1	51	3	AOUT1 SENSE
AOUT0	52	4	AOUT0 SENSE
AGND	53	5	AGND
AOUT7	54	6	AOUT7 SENSE
AOUT6	55	7	AOUT6 SENSE
AOUT5	56	8	AOUT5 SENSE
AOUT4	57	9	AOUT4 SENSE
AGND	58	10	AGND
NC	59	11	AGND(on J6)
NC	60	12	AGND(on J6)
NC	61	13	AGND(on J6)
NC	62	14	AGND(on J6)
AGND	63	15	AGND
NC	64	16	AGND(on J6)
NC	65	17	AGND(on J6)
NC	66	18	AGND(on J6)
NC	67	19	AGND(on J6)
AGND(on J8)	68	20	AGND
AGND(on J8)	69	21	AGND
AGND(on J8)	70	22	AGND
AGND(on J8)	71	23	AGND
AGND(on J8)	72	24	AGND
AGND(on J8)	73	25	AGND
AGND(on J8)	74	26	AGND
AGND(on J8)	75	27	AGND
AGND(on J8)	76	28	AGND
AGND(on J8)	77	29	AGND
AGND(on J8)	78	30	AGND
AGND(on J8)	79	31	AGND
AGND(on J8)	80	32	AGND
AGND(on J8)	81	33	AGND
AGND(on J8)	82	34	AGND
AGND(on J8)	83	35	AGND
DGND	84	36	DGND
EXT_TRIG	85	37	EXT_CMD
EXT_CLK	86	38	TMR2
TMR0	87	39	TMR1
DGND	88	40	DGND
DINO	89	41	DOUT0
DIN1	90	42	DOUT1
DIN2	91	43	DOUT2
DIN3	92	44	DOUT3
DIN4	93	45	DOUT4
DIN5	94	46	DOUT5
DIN6	95	47	DOUT6
DIN7	96	48	DOUT7



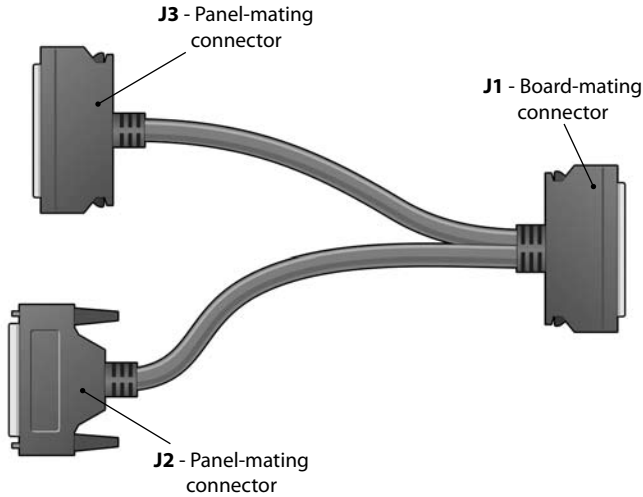
PDXI-AO-CBL-96

96-way, 3ft Y-split round shielded cable with molded covers

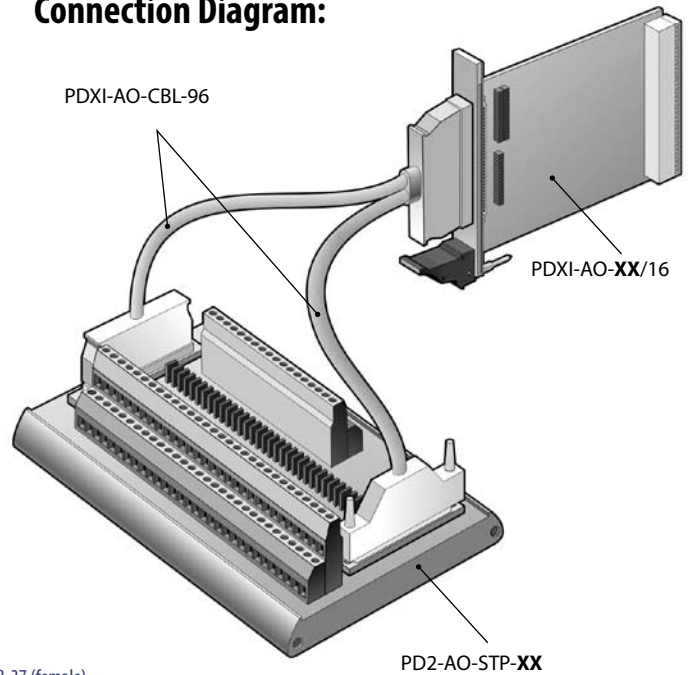
- Designed for PowerDAQ cPCI/PXI analog output cards (PDXI-AO-8/16, PDXI-AO-16/16, PDXI-AO-32/16)
- Carries up to 32 analog output lines, 8 digital input and 8 digital output lines
- Features 96-pin (pinless SCSI) female connector on the board-mating end
- Features 96-pin (pinless SCSI) and 37-pin (DB-37) female connectors on the panel-mating end



Layout:



Connection Diagram:



Pinout Diagrams:

J1* — pinless SCSI (female) 96-pin connector:

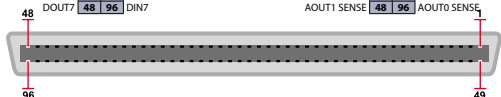
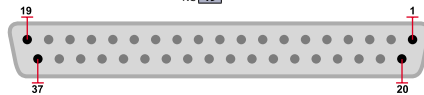
AOUT3 SENSE	1	49	AOUT3
AOUT2 SENSE	2	50	AOUT2
AOUT1 SENSE	3	51	AOUT1
AOUT0 SENSE	4	52	AOUT0
AGND2	5	53	AGND1
AOUT7 SENSE	6	54	AOUT7
AOUT6 SENSE	7	55	AOUT6
AOUT5 SENSE	8	56	AOUT5
AOUT4 SENSE	9	57	AOUT4
AGND4	10	58	AGND3
AOUT11 SENSE	11	59	AOUT11
AOUT10 SENSE	12	60	AOUT10
AOUT9 SENSE	13	61	AOUT9
AOUT8 SENSE	14	62	AOUT8
AGND6	15	63	AGND5
AOUT15 SENSE	16	64	AOUT15
AOUT14 SENSE	17	65	AOUT14
AOUT13 SENSE	18	66	AOUT13
AOUT12 SENSE	19	67	AOUT12
AGND7	20	68	AOUT16
AGND8	21	69	AOUT17
AGND9	22	70	AOUT18
AGND10	23	71	AOUT19
AGND11	24	72	AOUT20
AGND12	25	73	AOUT21
AGND13	26	74	AOUT22
AGND14	27	75	AOUT23
AGND15	28	76	AOUT24
AGND16	29	77	AOUT25
AGND17	30	78	AOUT26
AGND18	31	79	AOUT27
AGND19	32	80	AOUT28
AGND20	33	81	AOUT29
AGND21	34	82	AOUT30
AGND22	35	83	AOUT31
DGND2	36	84	DGND1
EXT CMD	37	85	EXT TRNG
TMR	38	86	EXT CLK
TMR1	39	87	TMR0
DGND4	40	88	DGND3
DOUT0	41	89	DINO
DOUT1	42	90	DINI1
DOUT2	43	91	DIN2
DOUT3	44	92	DIN3
DOUT4	45	93	DIN4
DOUT5	46	94	DIN5
DOUT6	47	95	DIN6
DOUT7	48	96	DIN7

J3* — pinless SCSI (female) 96-pin connector:

NC	1	49	NC
NC	2	50	NC
NC	3	51	NC
AGND1	4	52	NC
NC	5	53	AGND2
NC	6	54	AGND3
AOUT31	7	55	AOUT30
AOUT29	8	56	AOUT28
AOUT27	9	57	AOUT26
AOUT25	10	58	AOUT24
AGND4	11	59	AOUT23
AOUT22	12	60	AOUT21
AOUT20	13	61	AOUT19
AOUT18	14	62	AGND5
AOUT17	15	63	AOUT16
AOUT15	16	64	AOUT14
AOUT13	17	65	AOUT12
AGND6	18	66	AOUT11
AOUT10	19	67	AOUT9
AOUT8	20	68	AOUT7
AOUT6	21	69	AGND7
AOUT5	22	70	AOUT4
AOUT3	23	71	AOUT2
AOUT1	24	72	AOUT0
AGND9	25	73	AGND8
AGND11	26	74	AGND10
AGND13	27	75	AGND12
AGND15	28	76	AGND14
AGND17	29	77	AGND16
AGND18	30	78	NC
NC	31	79	NC
NC	32	80	AGND19
NC	33	81	NC
NC	34	82	NC
NC	35	83	NC
AGND20	36	84	NC
NC	37	85	NC
NC	38	86	NC
NC	39	87	AOUT15 SENSE
NC	40	88	AOUT14 SENSE
AOUT13 SENSE	41	89	AOUT12 SENSE
AOUT11 SENSE	42	90	AOUT10 SENSE
AOUT9 SENSE	43	91	AGND21
AOUT8 SENSE	44	92	AOUT7 SENSE
AOUT6 SENSE	45	93	AOUT5 SENSE
AOUT4 SENSE	46	94	AOUT3 SENSE
AGND22	47	95	AOUT2 SENSE
AOUT1 SENSE	48	96	AOUT0 SENSE

J2 — DB-37 (female) 37-pin connector:

DGND1	1	20	NC
TMR0	2	21	TMR2
NC	3	22	NC
NC	4	23	DGND2
TMR1	5	24	NC
DINO	6	25	DGND3
DINI	7	26	DOUT0
DIN2	8	27	DOUT1
DIN3	9	28	DOUT2
DIN4	10	29	DOUT3
DIN5	11	30	DOUT4
DIN6	12	31	DOUT5
DIN7	13	32	DOUT6
EXT TRNG	14	33	DOUT7
EXT CMD	15	34	NC
EXT CLK	16	35	DGND4
NC	17	36	NC
NC	18	37	NC
NC	19		



Note: Pinout is shown for the cable connected to 32-channel board (PDXI-AO-32/16). For 8- and 16-channel boards this diagram will change according to the pinout of the appropriate board's J1 connector.