

Microsys

User's Manual
CU824 Rev. 3
2nd edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
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Germany

declare that the product

CU824

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

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1. Introduction

1.1 Short Description

The **Single Euro** VMEbus board **CU824** is powered by the Motorola PowerPC **MPC8240**.

It features a **64 bit** wide data bus for the **32 (64/128) MByte SDRAM** area and the **two 8 MByte Flash** memory banks. The CU824 offers an optional **32 bit** wide **SRAM** area with battery backup.

The two onboard serial ports are handled via two **UARTs** with **16 Byte R/W-FIFO**.

The I²C-Interface of the MPC8240 controls a **512Byte EEPROM**, a **RTC** with battery backup and a **System Monitor** for supply voltage and temperature supervision.

The **PCI Interface** of the MPC8240 can be used for additional extensions. The local CPU bus as well as the PCI bus can be accessed via the VMEbus.

The VMEbus short I/O decoded **mailbox** with interrupt capability allows for process synchronization.

The **VMEbus interface** contains a single level arbiter and requester with a four level ROR option and a **7 level interrupt handler**.

The complete board is implemented in **CMOS technology**, which allows for a power consumption as low as: **5V / 5W @ 250 MHz** CPU speed.

The 5 volt board supply voltage is protected by a transient suppresser diode against overvoltage or wrong polarity.

The CU824 conforms to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297.

1.2 Options

- different DRAM sizes
- different FLASH memory sizes
- SRAM memory
- different PCI extensions

1.3 Specifications

The power requirements for the CU824 board are shown in the following table. The power consumption of the optionally used extension boards must be added to the given values.

Power Requirements:

+5V, +5%/-2.5%,	1.0A + used modules (typ. @250 MHz)
+12V, +5%/-2.5%	0mA + used modules
-12V, +5%/-2.5%	0mA + used modules

Environmental Requirements:

Operating Temperature	0 ° C to +70 ° C -40°C to +80°C optional
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

The CU824 can be supplied with single 5 volts, if no I/O module uses the 12 volts supply.

1.4 Related Documentation

The following manuals are applicable to the CU824:

- VMEbus Specification Manual ANSI/IEEE STD1014-1987
- MPC8240 RISC Microprocessor User's Manual
- ST16C2550 Dual UART Data Sheet
- LM81 System Hardware Monitor Data Sheet
- PCF8563 Real-time Clock Manual
- 24C164 EEPROM Data Sheet

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2. Delivery

2.1 Items shipped with this unit

- User's Manual CU824 Hardware
- MicroSys shipping carton



ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for CU824 installation

For installation of the CU824, the following items are required.

- Card cage or housing
- VMEbus motherboard
- Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V (+ 5 %, - 2,5 %),
- Unit requires optional +/-12V (+ 5 %, - 2,5 %),
- Mounted I/O-Modules may require +/-12V.
- Be sure voltage is of correct polarity.
- Unit should only be inserted into, and removed from card cage when power is off.
- Any modules must only be inserted or removed during power off.
- Check default jumper or switch setting.



cage must be well ventilated. The operating temperature must never exceed it's range. Never use the board without forced cooling!

**GUARANTEE IS VOID IF UNIT IS OPERATED
OUT OF IT'S SPECIFICATIONS!**

4. Board Overview

4.1 Features CU824

Board Format:	single eurocard format
Main Processor:	MPC8240 with PowerPC 603 Core 64 Bit Peripheral Bus 32 Bit PCI 2.1 Bus Interface 16 Kbyte instruction cache 16 Kbyte data cache onchip floating point unit up to 250MHz CPU core clock rate
Dynamic RAM:	four SDRAM devices 32 MByte capacity (optional 64MB or 128MB) 64 bit data bus width accessible by other VMEbus masters
Flash Memory:	two independent banks with burst capability 2 x 8 MByte capacity 64 bit data bus width accessible by other VMEbus masters single 5 volt programmable devices
Static RAM (optional):	512Kbyte or 2 MByte capacity 32 bit data bus width accessible by other VMEbus masters optional data backup with onboard battery and gold cap
EEPROM:	2KByte I ² C serial access device
Serial Interface:	ST16C2550 Dual UART 16 byte transmit FIFO 16 byte receive FIFO
Real Time Clock:	PCF8563 with time & date function backup function with onboard supply
Data backup:	short time backup via service free gold cap extended backup via 260mAh lithium cell external backup via VMEbus standby line
Front panel LEDs:	two user programmable LEDs
Front panel Keys:	RESET key for complete hardware reset
Temperature and Voltage Control:	LM81 hardware monitor for temperature and voltage control (LM35D processor temperature sensor)
Interrupt handler:	7 level onboard interrupt handler 7 level VMEbus interrupt handler software programmable VMEbus interrupt mask

System controller:	full VMEbus slot 1 functions single level arbiter single jumper function enable
VMEbus interface:	according to ANSI/IEEE STD1014-1987
VMEbus master:	DTB A16/A24 - D08(EO)/D16 VMEbus address modifier support standard and short I/O addressing dynamic bus sizing feature
VMEbus slave:	DTB A16 - D08(EO)/D16/ADO programmable VMEbus shared access base address programmable VMEbus shared access offset register
VMEbus mailbox:	programmable short I/O decoded 1KByte range autovector controlled local interrupt mode
VMEbus arbiter:	single level arbiter on level 3
VMEbus requester:	single level 2:1 pass requester release when done or 4 level release on request modes

5. Addressmap CU824

Type	Base	End	Select	Size
SDRAM Bank	\$0000 0000	\$01FF FFFF	local CS0	64Bit
Flash Memory Bank 1	\$FF00 0000	\$FF7F FFFF	local RCS1	64Bit
Flash Memory Bank 0	\$FF80 0000	\$FFFF FFFF	local RCS0	64Bit

VMEbus Std.Access	\$8000 0000	\$80FF FFFF	PCI-MEM	16Bit
SRAM Bank	\$8108 0000	\$810F FFFF	PCI-MEM	32Bit

Address Compare Register	\$FE80 0003		PCI-I/O	8Bit
VMEbus Interrupt Enable Register	\$FE80 0007		PCI-I/O	8Bit
Local Interrupt Enable Register	\$FE80 000B		PCI-I/O	8Bit
System Address Register	\$FE80 000F		PCI-I/O	8Bit
Board Control Register	\$FE80 0013		PCI-I/O	8Bit
VMEbus Interrupt Status Register	\$FE80 0017		PCI-I/O	8Bit
Local Interrupt Status Register	\$FE80 001B		PCI-I/O	8Bit
PCI Interrupt Status Register	\$FE80 001F		PCI-I/O	8Bit
Watchdog Retrigger Port	\$FE80 0023		PCI-I/O	---
Clear Mailbox Interrupt Register	\$FE80 0027		PCI-I/O	---
Board Revision Register	\$FE80 002B		PCI-I/O	8Bit
PLL State Register	\$FE80 002F		PCI-I/O	8Bit
Led Control Port	\$FE80 0033		PCI-I/O	8Bit
ST16C2550 UART Channel A	\$FE80 0080	\$FE80 00BF	PCI-I/O	8Bit
ST16C2550 UART Channel B	\$FE80 00C0	\$FE80 00FF	PCI-I/O	8Bit
VMEbus Short I/O	\$FE90 0000	\$FE7F FFFF	PCI-I/O	16Bit
VMEbus IACK Range	\$FEA0 0000	\$FEFF FFFF	PCI-I/O	16Bit

all shown addresses represent CPU side address ranges

24C164 EEPROM	\$B0	\$B1	I ² C-Bus	---
LM81 System Hardware Monitor	\$58	\$59	I ² C-Bus	---
PCF8563 Real Time Clock	\$A2	\$A3	I ² C-Bus	---



Attention !

The MPC8240 is configured at power up for address map B.

6. Functional Description

6.1 The MPC8240 Processor

The CU824 uses the MPC8240 PowerPC RISC microprocessor from Motorola. It can be configured for different CPU core and bus speed versions. The MPC8240 contains a 603e compatible core with 16 Kbyte data cache and 16 Kbyte instruction cache. It works on 3,3 volts bus supply and with 2,5 volts core supply voltage. The processor works with CPU clock rates from 99 up to 250MHz. The according local bus clock rate varies from 33 to 100MHz, while the PCI bus clock is sourced from a 33MHz oscillator. The desired clock configuration can be adjusted via the soldering link area PLL according to the following table.

PLL					MPC8240 - 250MHz		
1-2	3-4	5-6	7-8	9-10	PCI-Clock	Local Bus Clock	CPU-Clock
x	x	x	x	x	33MHz	99MHz	247,5MHz
x	---	x	x	x	33MHz	33MHz	99MHz
x	---	---	x	x	33MHz	66MHz	165MHz
x	---	---	---	x	33MHz	66MHz	198MHz
---	x	x	x	x	33MHz	99MHz	198MHz
---	x	---	x	x	33MHz	66MHz	231MHz
---	---	x	x	x	33MHz	82,5MHz	247,5MHz

(x = link installed / --- link not installed)

The local data bus is configured for **64 bit** for the SDRAM block connected to **CS0** and both Flash memory banks connected to **RCS0** and **RCS1**. All other select lines are not used on the local bus side of the MPC8240.

The **JTAG** interface of the CU824 can be used via the 16 pin standard wrap connector JTAG according to following table.

JTAG	Signal		Signal	JTAG
Pin 1	TDO		n.c.	Pin 2
Pin 3	TDI		TRST*	Pin 4
Pin 5	10K pullup		2K2 pullup	Pin 6
Pin 7	TCK		CKSTI	Pin 8
Pin 9	TMS		n.c.	Pin 10
Pin 11	SRST*		n.c.	Pin 12
Pin 13	DRST*		n.c.	Pin 14
Pin 15	10K pullup		GND	Pin 16

6.1.1 Board specific MPC8240 register values

Memory Control Configuration Register 1: **\$03D00000**

BIT Location:	Binary Value	Result:	Description:
ROMNAL	0000	30ns + 0x10ns	Flash Burst Cycle Length
ROMFAL	00111	30ns + 7x10ns	Flash Initial Cycle Length
DBUS-Size	10	64 Bit	SDRAM & Flash Bank A / B
ROM Burst	1	enable	Flash Burst Mode
MEMGO	(1)*	enable	Set to enable RAM interface
SREN	0	disable	SDRAM selfrefresh during sleep
RAM Type	0	SDRAM	FPM/EDO or SDRAM mode
PCKEN	0	disable	Parity Check
DRAM Bank 7	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 6	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 5	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 4	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 3	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 2	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 1	00	14 rows / 4 banks	SDRAM row address bit count
DRAM Bank 0	00	14 rows / 4 banks	SDRAM row address bit count

*** this bit must be set after complete configuration setting by a read modify write sequence !**

Memory Control Configuration Register 2: **\$0001800**

BIT Location:	Binary Value	Result:	Description:
TS wait timer	000	2x10ns	Flash data out disable time
AS ARISE time	0000	not used	AS falling edge of port X interface
AS AFALL time	0000	not used	AS rising edge of port X interface
ECC / Parity	0	not used	ECC or Parity Check mode
Write Parity Check	0	disabled	write parity error report function
Inline Parity Check	0	disabled	inline parity/ECC error report function
look aside ECC logic	0	disabled	FPM/EDO ram ECC function
EDO option	0	disabled	DRAM Extended data out
Refresh Interval	000110000000	15.5µsec	4096 cycles within 16ms
open page mode	0	4 open pages	3 or 4 open page DRAM mode
RMW parity	0	disabled	read modify write parity mode

Memory Control Configuration Register 3: **\$F2300000**

BIT Location:	Binary Value	Result:	Description:
Burst to precharge	1111	maximum	SDRAM open page time
refresh to active	0010	2x10ns	SDRAM refresh to activate command
RDLAT	0100	(3+1)x10ns	expected SDRAM CAS latency
CPX	0	disabled	extended SDRAM CAS write cycle
RAS low to CBR	0000	not used	FPM/EDO refresh timing
CAS low time	000	not used	FPM/EDO CAS access timing
CAS precharge	000	not used	FPM/EDO CAS access timing
CAS access time	000	not used	FPM/EDO CAS access timing
RAS/CAS delay	000	not used	FPM/EDO DRAM access timing
RAS precharge	000	not used	FPM/EDO RAS access timing

Memory Control Configuration Register 4: **\$253C322F**

BIT Location:	Binary Value	Result:	Description:
precharge to active	0010	2x10ns	SDRAM precharge to activate delay
active to precharge	0101	5x10ns	SDRAM activate to precharge delay
Burst Mode	0	4 beats	4 or 8 beat burst mode
INLINE	0	disabled	inline ECC/parity function
reserved	x		read value and write back
register mode	1	enabled	clocked data interface
burst to precharge	11	maximum	SDRAM open page time
reserved	xxx		read value and write back
registered DIMM	0	disabled	normal SDRAM mode
CAS latency	011	3x10ns	transferred to SDRAM at power up
sequential mode	0	enabled	sequential or interleaved mode
SDRAM burst length	010	4 beats	transferred to SDRAM at power up
active to read/write	0010	2x10ns	SDRAM activate to r/w command
burst to precharge	1111	maximum	SDRAM open page time

Clock Driver Control Register: \$0000

BIT Location:	Binary Value	Result:	Description:
PCI clock (0-4)	00000	enable	all PCI clocks active
reserved	xxx		read value and write back
SDRAM clock (0-3)	0000	enable	all SDRAM clocks active

Output Driver Control Register: \$FF

BIT Location:	Binary Value	Result:	Description:
DRV PCI	1	25 Ohms	PCI drive capability
DRV STD	1	20 Ohms	non PCI drive capability
DRV MEM CTRL	11	8/20 Ohms	memory driver capability
DRV PCI CLK	11	8 Ohms	PCI clock drive capability
DRV MEM CLK	11	8 Ohms	memory clock drive capability

Processor Interface Configuration Register 1: \$xx041CC

BIT Location:	Binary Value	Result:	Description:
reserved	xxxxxxxx		read value and write back
wait states	00	0	initial burst read waitstates
reserved	x		read value and write back
RCS0 state	read only	local ROM	power up reset configuration
reserved	x		read value and write back
processor type	read only	10	host processor type is 603
address map	read only	0	address map B is used
reserved	xxx		read value and write back
flash write enable	1	enabled	flash write mode
MCP enable	1	enabled	machine check assertion
reserved	x		read value and write back
DPARK	0	disabled	the data bus will not be parked to CPU
reserved	xx		read value and write back
store gathering	1	enabled	PCI buffer function
big endian mode	0	enabled	little or big endian mode
snoop loop	0	disabled	PCI to memory transaction snoop
APARK	0	disabled	the address bus will not be parked to CPU
PCI memory reads	11	enabled	speculative PCI reads from memory
reserved	xx		read value and write back

Processor Interface Configuration Register 2: \$04040004

BIT Location:	Binary Value	Result:	Description:
reserved	xx		read value and write back
PCI serialize flag	0	enabled	serialized PCI configuration writes
reserved	x		read value and write back
snoop enable	0	enabled	PCI to local memory snoop function
ROM remapping	1	local	all ROM/Flash accesses on local bus
Flash write lock	0	disabled	Flash writes are enabled
reserved	xxxxx		read value and write back
snoop wait states	01	1 waitsate	snoop waitstate count
reserved	xxxxxxxxxxxx x		read value and write back
address phase waits	01	1 waitstate	address phase waitstate count
reserved	xx		read value and write back



**For detailed chip information see
Technical manual MPC8240**

6.2 Memory

6.2.1 The DRAM Area

The CU824 is fitted out with four synchronous dynamic ram devices which allows for a total capacity of 32MByte, 64MByte or 128MByte depending on the used chip sizes. The ram bank is directly controlled by the CS0 select line of the MPC8240. The DRAM data port is 64 bits wide and no parity check is performed. The SDRAM contains 4 banks and supports auto refresh and selfrefresh with 4096 cycles during 64ms. It is organized with 12 row and 8 column addresses. The pins of the SDRAM device are controlled by the MPC8240 according to following table.

SDRAM	MPC8240	Description
A0-A9	SDMA12-SDMA3	address
A10/AP	SDMA2	address/auto precharge
A11	SDMA1	address
A12	SDMA0/SDBA1	address
BA0	SDBA0	bank address 0
BA1	SDMA0/SDBA1	bank address 1
CLK	SDRAM-CLK-0	clock
CLKE	CKE	clock enable
UDQM	SDQMx	upper data I/O mask
LDQM	SDQMy	lower data I/O mask
RAS	SDRAS	row address strobe
CAS	SDCAS	column address strobe
CS	RAS/CS-0	chip select
WE	WE	write enable



For detailed information about the SDRAM chip specification, please refer to the according SDRAM data sheet.

6.2.2 The Flash Memory

The flash memory area of the CU824 consists of two banks with a total capacity of 16Mbyte. The Flash bank A is controlled via the RCS0 line of the MPC8240, the Flash bank B via the RCS1 line. The data bus is 64bits wide and no parity check is performed. The data lanes of all devices are swapped according to the necessary endian conversion. The WAIT pin is not connected and left floating. The ADV pin is not connected and left floating. The ADV pin can either be connected to ground or to the CE line, in case the burst mode should be used or not. Bank A works in normal mode if the soldering link FA is set to position 2-3, which connects the ADV pin to ground. Bank B is controlled by soldering link FB in the same manner. Position 1-2 of FA and FB connects the ADV pin to the CE pin of each bank. The pins of the Flash devices are controlled by the MPC8240 according to following table.

Flash Bank A	MPC8240	Description
A0-A10	SDMA12-SDMA2	address
A11-A19	AR7-AR0	address
CLK	SDRAM-CLK-1	clock
CE	RCS0	chip select
OE	FOER	output enable
ADV	RCS0 or GND	address valid
WE	WE via BCR-D1	write enable
RST	HRST	hard reset
WP	via BCR-D0	write protect
D0-D15	D15-D0	endian swapped data lanes

Flash Bank B	MPC8240	Description
A0-A10	SDMA12-SDMA2	address
A11-A19	AR7-AR0	address
CLK	SDRAM-CLK-2	clock
CE	RCS1	chip select
OE	FOER	output enable
ADV	RCS1 or GND	address valid
WE	WE via BCR-D2	write enable
RST	HRST	hard reset
WP	via BCR-D0	write protect
D0-D15	D15-D0	endian swapped data lanes



To protect the Flash memory contents against unattended write cycles, a security function has been implemented.

The Board Control Register at location \$FE800013 allows a complete protection against all write accesses to one or both banks of the flash devices. The BCR contains three protection bits, one for each bank write line (WE) and one for the write protect pin (WP) of both Flash banks. The BCR can be read back for verification. After a reset, these bits are set to low and the write protect mode is activated.

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset	0	0	0	0	0	0	0	0
Flash Bank 0/1 WP Pin = 1	x	x	x	x	x	x	x	0
Flash Bank 0/1 WP Pin = 0	x	x	x	x	x	x	x	1
Flash-Bank 0 write disable	x	x	x	x	x	x	0	x
Flash-Bank 0 write enable	x	x	x	x	x	x	1	x
Flash-Bank 1 write disable	x	x	x	x	x	0	x	x
Flash-Bank 1 write enable	x	x	x	x	x	1	x	x



For detailed chip information see Technical manual of Intel 28F160F3B flash memory products.

6.2.3 The Static RAM Area

Optionally, the CU824 contains a static ram area consisting of 4 SRAM devices with either 128Kx8 or 512Kx8 capacity, which allows for a total capacity of 512KByte or 2MByte at a 32 bit wide data bus. The SRAM is located on the PCI bus side of the MPC8240 within the PCI memory range at the base address \$01000000 and is decoded up to \$01FFFFFF. The small devices must be addressed with A19 set to high, i.e. from \$01080000 to \$010FFFFFF. The large SRAM devices got no restrictions and appear several times within the complete address range. It responds as a non-burstable, medium fast 32 bit PCI device with a target disconnect after 2 clock cycles within a frame at 33MHz PCI clock speed. It does neither support parity generation nor detect any parity error messages on the PERR or SERR lines.

The contents of the SRAM area is protected against data loss by a backup circuitry. The backup power is supplied by a service free gold capacitor or a lithium cell. An extended backup time can be reached, if the VMEbus standby line on ST1B pin 31 is used to supply the necessary backup power. In any case, the backup time mainly depends on the used SRAM devices and their standby power consumption. The backup feature of the CU824 cannot be disabled. The backup power is supplied to the SRAM area as well as to the onboard real time clock.

6.3 The Serial I/O-Interface

6.3.1 The ST16C2550 Dual UART

The CU824 contains a ST16C2550 Dual UART device. The UART supports two I/O channels with a 16 byte receive and a 16 byte transmit FIFO. The UART is addressed within the PCI I/O access range as an 8 bit device on the PCI data path D24 to D31 according to following address map. The UART offers two interrupt lines sourced to the MPC8240 IRQ2 line if the according enable bits within the (L)ocal (I)nterrupt (E)nable (R)egister at location \$FE80000B are set. The status of these interrupt lines is reflected within the (L)ocal (I)nterrupt (S)tatus register at location \$FE80001B independent of the enable bit state. The UART device is supplied with an external clock of 7.3728MHz which allows for data rates up to 460.8Kbps.

Both channels are accessible via two frontpanel connectors. The desired EIA interface standard of both ports can be individually realized by two I/O modules of various types.

UART channel A:

address	read mode		write mode	
\$FE800083	receive holding register	RHR	THR	transmit holding register
\$FE800087			IER	interrupt enable register
\$FE80008B	interrupt status register	ISR	FCR	FIFO control register
\$FE80008F			LCR	line control register
\$FE800093			MCR	modem control register
\$FE800097	line status register	LSR		
\$FE80009B	modem status register	MSR		
\$FE80009F	scratchpad register	SPR	SPR	scratchpad register

UART channel B:

address	read mode		write mode	
\$FE8000C3	receive holding register	RHR	THR	transmit holding register
\$FE8000C7			IER	interrupt enable register
\$FE8000CB	interrupt status register	ISR	FCR	FIFO control register
\$FE8000CF			LCR	line control register
\$FE8000D3			MCR	modem control register
\$FE8000D7	line status register	LSR		
\$FE8000DB	modem status register	MSR		
\$FE8000DF	scratchpad register	SPR	SPR	scratchpad register

Bit map of the (L)ocal (I)nterrupt (E)nable register:

LIE @ \$FE80000B	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABIE	MBIE	SAIE	SBIE	P3IE	P2IE	P1IE	P0IE
reset state	0	0	0	0	0	0	0	0
PCI-IRQ0 enabled	x	x	X	X	x	x	x	1
PCI-IRQ1 enabled	x	x	X	X	x	x	1	x
PCI-IRQ2 enabled	x	x	X	X	x	1	x	x
PCI-IRQ3 enabled	x	x	X	X	1	x	x	x
SIO-B IRQ enabled	x	x	X	1	x	x	x	x
SIO-A IRQ enabled	x	x	1	X	x	x	x	x
Mailbox IRQ enabled	x	1	X	X	x	x	x	x
Abort Key & VMEbus ACFail enabled	1	x	X	X	x	x	x	x

Bit map of the (L)ocal (I)nterrupt (S)tatus register:

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
Watchdog Reset occurred	x	x	X	X	x	x	x	0
VMEbus ACFail active	x	x	X	X	x	x	0	x
RTC IRQ active	x	x	X	X	x	0	x	x
LM81 IRQ active	x	x	X	X	0	x	x	x
SIO-B IRQ active	x	x	X	0	x	x	x	x
SIO-A IRQ active	x	x	0	X	x	x	x	x
Mailbox IRQ active	x	0	X	X	x	x	x	x
Abort Key IRQ	0	x	X	X	x	x	x	x



**For detailed programming information and chip description,
please refer to ST16C2550 Data Sheet !**

6.3.2 The EIA Module Sockets

The CU824 offers two 22 pin sockets for various types of I/O modules. The modules connect the UART I/O signals to the frontpanel connectors according to following table. The frontpanel connectors can be either populated with 9 pin DSUB or 8 pin RJ45. The ground lines of both channels are protected against overcurrent by 100mA rated silicon fuses.

UART	Module Pin	Direction	Module Pin	DSUB	RJ45
		GND	3	5	3
RI	6	<---	5	9	---
DTR	4 & 8	--->	7	4	8
CTS	10	<---	9	8	7
TXD	12	--->	11	3	4
RTS	14	--->	13	7	2
RXD	16	<---	15	2	5
DSR	18	<---	17	6	1
DCD	20	<---	19	1	6

6.4 The I²C Bus

The I²C bus onboard the CU824 is controlled via the SDA and SCL pins of the MPC8240 and contains a real-time clock, an EEPROM and a system hardware monitor device.

6.4.1 The EEPROM

The CU824 offers a 16KBit serial EEPROM for storing system or board parameters. The 24C164 device is internally organized to 2048 x 8 bit and allows for at least 100000 write cycles with a typical cycle time of 5ms.

The 24C164 device responds on the I²C bus at address \$B1 for read and \$B0 for write accesses.



**For detailed programming information and chip description,
please refer to 24C164 Data Sheet !**

6.4.2 The Real Time Clock

The PCF8563 RTC features a clock function with a calendar and an universal timer with alarm and interrupt function. The RTC is protected against data loss by a backup circuitry. The backup feature supplied from a service free gold capacitor cannot be disabled. For long time applications the VMEbus standby line on ST1B pin 31 can be used to supply the necessary backup power. The maskable interrupt can be generated on the MPC8240 IRQ line 4 if the according enable bit within the BCR at location \$FE800013 is set to high. The BCR contents is cleared after reset and can be read back for verification. The current status of the LM81 interrupt line can be detected within the LIS register at location \$FE80001B.

The RTC device responds on the I²C bus at address \$A3 for read and \$A2 for write accesses.

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset	0	0	0	0	0	0	0	0
RTC IRQ disabled	x	0	x	x	x	x	x	x
RTC IRQ enabled	x	1	x	x	x	x	x	x

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
RTC IRQ active	x	x	x	x	x	0	x	x
RTC IRQ inactive	x	x	x	x	x	1	x	x



**For detailed programming information and chip description,
please refer to Philips PCF8563 Data Sheet !**

6.4.3 The System Hardware Monitor

The board ambient and supply conditions of the CU824 can be sensed by the microprocessor system hardware monitor LM81. It offers the monitoring of the board ambient temperature, all board supply voltages, the onboard battery condition and the voltage range of an external battery. The VID0-4 inputs are used to monitor the current PLL configuration of the MPC8240. A maskable interrupt can be generated on the MPC8240 IRQ line 4 if the according enable bit within the BCR at location \$FE800013 is set to high. The BCR content is cleared after reset and can be read back for verification. The current status of the LM81 interrupt line can be detected within the LIS register at location \$FE80001B.

The LM81 device responds on the I²C bus at address \$59 for read and \$58 for write accesses.

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset	0	0	0	0	0	0	0	0
LM81 IRQ disabled	0	x	x	x	x	x	x	x
LM81 IRQ enabled	1	x	x	x	x	x	x	x

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
LM81 IRQ active	x	x	x	x	0	x	x	x
LM81 IRQ inactive	x	x	x	x	1	x	x	x

The pins of the LM81 are connected according to following table.

connected to:	LM81		connected to:
pulldown to ground	A0/NT0	VID0	PLL0
pulldown to ground	A1	VID1	PLL1
CPU-SDA	SMBdata	VID2	PLL2
CPU-SCL	SMBclock	VID3	PLL3
not used and left open	FAN1	VID4	PLL4
not used and left open	FAN2	Vccp1	(U+Uf)/2 of local battery
not used and left open	CI	+2.5V _{in}	VEE = 2.5V for CPU Core
not used and left open	OVTA	+3.3V _{in}	VDD = 3.3V for CPU & Logic
3.3V supply	V+	+5.0V _{in}	VCC = 5V for Logic
CPU-IRQ	INT	+12V _{in}	+12V for PCI bus
not used and left open	DACO/NTI	Vccp2	2*U of temperature sensor LM35D
CPU-Reset	RESET	GND	ground

The voltage detection of the local battery is handled via a very low current forward biased diode. The U_f of the used diode is slightly temperature dependent and decreases at a high ambient temperature nearly to zero. At a low ambient temperature, the U_f reaches values up to 200mV. If necessary, a simple correction might be used to keep the measuring error below that value.

The CU824 contains the LM35D temperature sensor from National Semiconductor. It features a 10mV/°C output which is multiplied by 2 and connected to the Vccp2 input of the LM81, i.e. 20mV/°C within the range from 0°C up to 150°C. The sensor is mounted on the top side of the processor heat sink.

The PLL configuration is reflected via the VID0 to VID4 inputs according to following table.

PLL					MPC8240 - 250MHz		
0	1	2	3	4	PCI-Clock	Local Bus Clock	CPU-Clock
L	L	L	L	L	33MHz	99MHz	247,5MHz
L	H	L	L	L	33MHz	33MHz	99MHz
L	H	H	L	L	33MHz	66MHz	165MHz
L	H	H	H	L	33MHz	66MHz	198MHz
H	L	L	L	L	33MHz	99MHz	198MHz
H	L	H	L	L	33MHz	66MHz	231MHz
H	H	L	L	L	33MHz	82,5MHz	247,5MHz

(L = LOW / H = HIGH)



**For detailed programming information and chip description,
please refer to LM81 Data Sheet !**

6.5 Miscellaneous

6.5.1 The Backup Feature

The backup feature of the CU824 is used to protect the **RTC** as well as the **SRAM** area. Both devices are connected to the MAX-791, which controls the backup supply and the power up and down sequences to avoid unintended write pulses. The backup power is supplied by a **service free gold capacitor** as well as by a **260mAh lithium cell** (CR2430). In case the cell must be replaced, the goldcap will avoid data loss of the connected devices. The RTC as well as the SRAM area cannot be disconnected from the backup power.

The gold capacitor allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended the backup power can be supplied via the onboard lithium cell or via the VMEbus standby line on connector ST1A, pin 31. The external supply voltage should not exceed 5,25 volts and not fall below 2.5 volts to ensure correct data retention.

The power consumption table of all backup connected devices:

device:	max.current:	total:
MAX791	5 μ A	5 μ A
PCF8563	0,5 μ A @ 5volts	0,5 μ A
KM684000ALG-5L	50 μ A @ 3volts	200 μ A

The MAX791 also features a low battery monitor function. During a power up or a key reset period, the battery voltage is sampled and, in case it is detected below 2V, any second access to the SRAM area will be inhibited. The function allows the user to detect a low battery state by two write accesses to a certain location of the SRAM area. If the first pattern, f.e. \$00, is written and the second pattern, f.e. \$FF, is allowed or inhibited by the MAX791, the user can detect the battery condition by the contents of the previous written RAM cell, i.e. \$FF for o.k. and \$00 for a low battery.

6.5.2 The Board Reset Function

During power up or power down sequences, the board supervisory circuit MAX-791 activates the board reset line and holds the CU824 in a defined state. The reset line will be low for at least 200ms if the supply voltage reaches 4.65 volts. Below that voltage, the reset line will be continuously low. If the board is configured as system controller, the VMEbus reset line driver will be activated as well. The board reset function controls all onboard devices and logic with the exception of the board and VMEbus clock generation.

6.5.3 Board Revision Register

For software adoption, the CU824 contains a (B)oard (R)evision (R)egister, which can be read out at location \$FE80002F.

BRR @ \$FE80002F	D7	D6	D5	D4	D3	D2	D1	D0
Revision 2	0	0	0	0	0	0	1	0

6.5.4 PLL State Register

The PLL state register reflects the 5 Bit setting of the soldering link area PLL for the MPC8240 clock configuration. This setting can also be read out via the system hardware monitor.

PLL @ \$FE80002F	D7	D6	D5	D4	D3	D2	D1	D0
read only	0	0	0	PLL0	PLL1	PLL2	PLL3	PLL4

PLL					MPC8240 - 250MHz		
0	1	2	3	4	PCI-Clock	Local Bus Clock	CPU-Clock
L	L	L	L	L	33MHz	99MHz	247,5MHz
L	H	L	L	L	33MHz	33MHz	99MHz
L	H	H	L	L	33MHz	66MHz	165MHz
L	H	H	H	L	33MHz	66MHz	198MHz
H	L	L	L	L	33MHz	99MHz	198MHz
H	L	H	L	L	33MHz	66MHz	231MHz
H	H	L	L	L	33MHz	82,5MHz	247,5MHz

(L = LOW / H = HIGH)

6.5.5 The LED Control Port

The CU824 offers two user LEDs, which are switched on during any power up or key reset. The state of these two user LEDs can be changed by the LED control port at the address location \$FE800033 via the data lines D1 and D0. The two control bits can be read back for verification. All other bits can not be set and are always read as zero.

LCP @ \$FE800033	D7	D6	D5	D4	D3	D2	D1	D0
reset state	0	0	0	0	0	0	0	0
user LED 1 on	0	0	0	0	0	0	X	1
user LED 1 off	0	0	0	0	0	0	X	0
user LED 2 on	0	0	0	0	0	0	1	X
user LED 2 off	0	0	0	0	0	0	0	X

6.5.6 Hardware Watchdog Timer

The CU824 features a fixed rate hardware timer for watchdog purposes, which can be enabled by software. Once enabled, it only can be disabled by a hardware reset. The time out rate is set to 1.6 seconds. Within that time at least one read access must be performed to the (W)atchdog (R)etrigger (R)egister, located at \$FE800023, to retrigger the timer. The enable function is performed within the (B)oard (C)ontrol (R)egister at location \$FE800013. The time out sequence can be modified by an additional hardware component on the SMD-0805 location C6 according to following equation:

$$\text{Watchdog Time-out Period in ms} = 2.1 \times (\text{capacitor C6 value in nF})$$

(allowed values are 4,7nF to 100nF)

In case a reset has been issued by the watchdog timer, the WDEN bit within the BCR is cleared, the watchdog is disabled and the WDGO bit within the (L)ocal (I)nterrupt (S)tatus register is set.

Bit map of the (B)oard (C)ontrol (R)egister:

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset	0	0	0	0	0	0	0	0
Watchdog enabled	x	x	1	x	x	x	x	x

The watchdog timer must reset within the given time-out period by a read access to the (W)atchdog (R)etrigger (R)egister located at \$FE800023. A write access to the given address will reset the WDGO watchdog status bit within the (L)ocal (I)nterrupt (S)tatus register. This status bit is not defined after power up, and may have any state. Therefore, it is necessary to initialize this status bit by a software routine, which is able to distinguish between a power up reset and a reset during normal operation.

WDR @ \$FE800023	D7	D6	D5	D4	D3	D2	D1	D0
read/write	---	---	---	---	---	---	---	---

Bit map of the (L)ocal (I)nterrupt (S)tatus register:

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
Normal Reset occurred	x	x	x	x	x	x	x	0
Watchdog Reset occurred	x	x	x	x	x	x	x	1

6.6 Interrupt Structure

6.6.1 The Interrupt Structure

The CU824 offers a bit maskable 7 level VMEbus interrupt handler and an 11 source onboard interrupt structure. The 7 VMEbus interrupt levels work in vector controlled mode only, while the onboard interrupts do not support any vector. The interrupt priority structure of the VMEbus must be realized by software, i.e. by the use of mask and status register bits for each VMEbus interrupt level. The interrupt prioritisation of all local interrupt sources can be freely handled according to the users' demands.

6.6.2 The VMEbus Interrupt Handler

Each VMEbus interrupt level can be enabled or disabled by software via the (V)MEbus (I)nterrupt (E)nable register at location \$FE800007. After a hardware reset all bits of this register are set to zero and all VMEbus interrupt levels are disabled. **To enable** a VMEbus interrupt level the according bit must be **set to high**. The register contents can be read back for verification.

VIE @ \$FE800007	D7	D6	D5	D4	D3	D2	D1	D0
read/write	VIER7	VIER6	VIER5	VIER4	VIER3	VIER2	VIER1	---
reset state	0	0	0	0	0	0	0	0
VME-IRQ1 enable	x	x	x	x	x	x	1	x
VME-IRQ2 enable	x	x	x	x	x	1	x	x
VME-IRQ3 enable	x	x	x	x	1	x	x	x
VME-IRQ4 enable	x	x	x	1	x	x	x	x
VME-IRQ5 enable	x	x	1	x	x	x	x	x
VME-IRQ6 enable	x	1	x	x	x	x	x	x
VME-IRQ7 enable	1	x	x	x	x	x	x	x

All VMEbus interrupt lines share the MPC8240 interrupt line IRQ3.

The current state of each VMEbus interrupt line can be checked within the (V)MEbus (I)nterrupt (S)tatus register at location \$FE800017. The low active status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

VIS @ \$FE800017	D7	D6	D5	D4	D3	D2	D1	D0
read/write	VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	ARBE
VME-IRQ1 active	x	x	x	x	x	x	0	x
VME-IRQ2 active	x	x	x	x	x	0	x	x
VME-IRQ3 active	x	x	x	x	0	x	x	x
VME-IRQ4 active	x	x	x	0	x	x	x	x
VME-IRQ5 active	x	x	0	x	x	x	x	x
VME-IRQ6 active	x	0	x	x	x	x	x	x
VME-IRQ7 active	0	x	x	x	x	x	x	x

The necessary VMEbus acknowledge procedure must be performed by a **read** access within the PCI-I/O address range from \$FEA00000 to \$00BFFFFFF. The data byte transferred on the data line AD31 to AD24 during the acknowledge cycle can be used to distinguish between different interrupt sources on the same VMEbus interrupt level. In order to meet the VMEbus specifications, the necessary acknowledge cycles must be performed according to following table.

VMEbus Interrupt Acknowledge Access Address Overview:

IACK for level	VA3	VA2	VA1	Access Address	Command
VME-IRQ1	0	0	1	\$FEA0 0003	Byte Read
VME-IRQ2	0	1	0	\$FEA0 0005	Byte Read
VME-IRQ3	0	1	1	\$FEA0 0007	Byte Read
VME-IRQ4	1	0	0	\$FEA0 0009	Byte Read
VME-IRQ5	1	0	1	\$FEA0 000B	Byte Read
VME-IRQ6	1	1	0	\$FEA0 000D	Byte Read
VME-IRQ7	1	1	1	\$FEA0 000F	Byte Read

6.6.3 The Onboard Interrupt Handler

There are 11 low active interrupt sources onboard the CU824. Each source can be enabled or disabled individually by software and its current status can be checked within two status registers. After a hardware reset all bits of the enable registers are set to zero and all local interrupt sources are disabled. **To enable** an interrupt source the according bit must be **set to high**. The register contents can be read back for verification.

Bit map of the (L)ocal (I)nterrupt (E)nable register:

LIE @ \$FE80000B	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABIE	MBIE	SAIE	SBIE	P3IE	P2IE	P1IE	P0IE
reset state	0	0	0	0	0	0	0	0
PCI-IRQ0 enabled	x	x	x	x	x	x	x	1
PCI-IRQ1 enabled	x	x	x	x	x	x	1	x
PCI-IRQ2 enabled	x	x	x	x	x	1	x	x
PCI-IRQ3 enabled	x	x	x	x	1	x	x	x
SIO-B IRQ enabled	x	x	x	1	x	x	x	x
SIO-A IRQ enabled	x	x	1	x	x	x	x	x
Mailbox IRQ enabled	x	1	x	x	x	x	x	x
Abort Key & VMEbus ACFail enabled	1	x	x	x	x	x	x	x

Bit map of the (B)oard (C)ontrol (R)egister:

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset state	0	0	0	0	0	0	0	0
RTC IRQ enabled	x	1	x	x	x	x	x	x
LM81 IRQ enabled	1	x	x	x	x	x	x	x

The current state of each local interrupt source can be checked within the (L)ocal (I)nterrupt (S)tatus register at location \$FE80001B and the (P)CI (I)nterrupt (S)tatus register at location \$FE80001F. The low active status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

Bit map of the (L)ocal (I)nterrupt (S)tatus register:

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
Watchdog Reset occurred	x	x	x	x	x	x	x	0
VMEbus ACFail active	x	x	x	x	x	x	0	x
RTC IRQ active	x	x	x	x	x	0	x	x
LM81 IRQ active	x	x	x	x	0	x	x	x
SIO-B IRQ active	x	x	x	0	x	x	x	x
SIO-A IRQ active	x	x	0	x	x	x	x	x
Mailbox IRQ active	x	0	x	x	x	x	x	x
Abort Key IRQ	0	x	x	x	x	x	x	x

Bit map of the (P)CI (I)nterrupt (S)tatus register:

PIS @ \$FE80001F	D7	D6	D5	D4	D3	D2	D1	D0
read only	1	1	1	1	IRP3	IRP2	IRP1	IRP0
PCI-IRQ0 active	1	1	1	1	x	x	x	0
PCI-IRQ1 active	1	1	1	1	x	x	0	x
PCI-IRQ2 active	1	1	1	1	x	0	x	x
PCI-IRQ3 active	1	1	1	1	0	x	x	x

The interrupt structure of the MPC8240 is realized according to following table.

MPC8240	External Source
IRQ0	Abort Key / VMEbus ACFail
IRQ1	PCI-IRQ(0-3)
IRQ2	SIO-A / SIO-B
IRQ3	VMEIRQ(1-7)
IRQ4	Mailbox / LM81 / RTC

By reprogramming the content of the ispLSI device, other combinations of the given interrupt sources and the MPC8240 interrupt lines IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 can be realized.

6.7 The VMEbus Interface

The VMEbus interface of the CU824 is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 rows A, B and C contain all standard VMEbus lines, necessary for A16/A24, D8/D16 master/slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM0 to AM5 are a part of the VMEbus specifications and serve to differentiate between certain memory areas. All address modifier lines are necessary for the mailbox and the shared access decoding logic. The CU824 accepts only slave data accesses within the VMEbus short I/O range and the VMEbus standard access area.

The following AM-Codes are accepted by the CU824:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low

H = logical high

The following AM-Codes are generated by the CU824:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	H	L	Standard Supervisory Prog.	(3E)
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low

H = logical high

6.7.1 Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	(BCLR*)	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	UDS*	BR0*	SYSRESET*
13	LDS*	BR1*	LWORD*
14	RW*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	not connected	A17
22	IACKOUT*	not connected	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	5VSTB	+12V
32	+5V	+5V	+5V

(signals enclosed in brackets are not used and left open)

6.7.2 The VMEbus Shared Access Decoding:

The local and the PCI bus system of the CU824 including all its devices and memories can be accessed by any other VMEbus master. The necessary access address from the VMEbus side is decoded, masked and enabled by internal registers of the onboard ispLSI. Any shared access from the VMEbus side must be performed with the proper address modifier combination for a standard data access and the state of each compare bit must match with the state of the according VMEbus address line. The VMEbus address lines VME A22 and VME A21 are always decoded to zero, i.e. the decoded window size is set to 1MByte with 4MByte programmable address steps. The enable bit ACR5 within the (S)hared (A)ddress (C)ompare register at location \$FE800003 allows the access to be enabled or disabled. The remaining register bits from ACR4 to ACR0 are used for the mailbox decoding within the VMEbus Short I/O range. Because the VMEbus standard access sources only address lines up to A23, the missing upper 8 address lines for a proper 32 bit PCI address decoding must be generated by an additional register. Therefore, the eight bit wide (S)hared (A)ccess (A)ddress register issues its contents to the PCI address lines AD24 to AD31 during any shared access. After a manual or VMEbus reset, all bits are cleared and the shared access is disabled at all.

The following AM-Codes are necessary for the shared access:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)

L = logical low

H = logical high

Bit map of the (S)hared (A)ccess (A)ddress register:

SAA @ \$FE8000F	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	SAR0
reset state	0	0	0	0	0	0	0	0
sources PCI address	AD31	AD30	AD29	AD28	AD27	AD26	AD25	AD24

Bit map of the (S)hared (A)ddress (C)ompare register:

SAC @ \$FE80003	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ACR7	ACR6	ACR5	ACR4	ACR3	ACR2	ACR1	ACR0
reset state	0	0	0	0	0	0	0	0
compared with	VME A23	VME A22	1	1	VME A15	VME A14	VME A13	VME A12
disabled	x	x	0	x	x	x	x	x
\$000000-\$0FFFFFF	0	0	1	x	x	x	x	x
\$400000-\$4FFFFFF	0	1	1	x	x	x	x	x
\$800000-\$8FFFFFF	1	0	1	x	x	x	x	x
\$C00000-\$CFFFFFF	1	1	1	x	x	x	x	x

ACR7	VMEbus Shared Access Address Compare Bit for VA23	state compare
ACR6	VMEbus Shared Access Address Compare Bit for VA22	state compare
ACR5	VMEbus Shared Access Enable Bit	high active



The address range of the onboard addressed device cannot be shifted or manipulated by the used VMEbus base address, i.e. the local access address of the PCI device or the MPC8240 local bus device must match with the SAA and SAC programmed register contents.

6.7.3 The VMEbus Mailbox

The mailbox feature of the CU824 is realized by a programmable location monitor function within the VMEbus short I/O range. The mailbox feature covers 1KByte of the VMEbus short I/O range. The programmable base address decodes the VMEbus address lines from VME A15 down to VME A10 and all VMEbus address modifiers. The address lines VME A10 and VME A11 are always decoded to zero. The according enable and compare bits are located within the (S)hared (A)ddress (C)ompare register at \$FE800003. The mailbox issues an interrupt on level 4 if a byte or word sized access is performed within the programmed address range. The mailbox interrupt function must be enabled within the (L)ocal (I)nterrupt (E)nable register at location \$FE80000B. If the enable bit is set to high, the mailbox function is enabled and a mailbox interrupt can be generated. The interrupt will be held active as long as this bit is in a high state or the (C)lear (M)ailbox (I)nterrupt register at location \$FE800027 has been accessed. The actual state of the mailbox interrupt signal is reflected within the (L)ocal (I)nterrupt (S)tatus register at location \$FE80001F. After a reset the according compare and enable bits are set to zero and the mailbox interrupt is disabled.

Bit map of the (C)lear (M)ailbox (I)nterrupt register:

CMI @ \$FE800027	D7	D6	D5	D4	D3	D2	D1	D0
read/write	---	---	---	---	---	---	---	---

Bit map of the (L)ocal (I)nterrupt (S)tatus register:

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
Mailbox IRQ active	x	0	x	x	x	x	x	x
Mailbox IRQ inactive	x	1	x	x	x	x	x	x

Bit map of the (L)ocal (I)nterrupt (E)nable register:

LIE @ \$FE80000B	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABIE	MBIE	SAIE	SBIE	P3IE	P2IE	P1IE	P0IE
reset state	0	0	0	0	0	0	0	0
Mailbox IRQ enabled	x	1	x	x	x	x	x	x
Mailbox IRQ disabled	x	0	x	x	x	x	x	x

Bit map of the (S)hared (A)ddress (C)ompare register:

SAC @ \$FE800003	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ACR7	ACR6	ACR5	ACR4	ACR3	ACR2	ACR1	ACR0
reset state	0	0	0	0	0	0	0	0
compared with	VME A23	VME A22	1	1	VME A15	VME A14	VME A13	VME A12
disabled	x	x	x	0	x	x	x	x
\$0000-\$03FF	x	x	x	1	0	0	0	0
\$1000-\$13FF	x	x	x	1	0	0	0	1
\$2000-\$23FF	x	x	x	1	0	0	1	0
\$3000-\$33FF	x	x	x	1	0	0	1	1
\$4000-\$43FF	x	x	x	1	0	1	0	0
\$5000-\$53FF	x	x	x	1	0	1	0	1
\$6000-\$63FF	x	x	x	1	0	1	1	0
\$7000-\$73FF	x	x	x	1	0	1	1	1
\$8000-\$83FF	x	x	x	1	1	0	0	0
\$9000-\$93FF	x	x	x	1	1	0	0	1
\$A000-\$A3FF	x	x	x	1	1	0	1	0
\$B000-\$B3FF	x	x	x	1	1	0	1	1
\$C000-\$C3FF	x	x	x	1	1	1	0	0
\$D000-\$D3FF	x	x	x	1	1	1	0	1
\$E000-\$E3FF	x	x	x	1	1	1	1	0
\$F000-\$F3FF	x	x	x	1	1	1	1	1

ACR4	VMEbus Mailbox Access Enable Bit	high active
ACR3	VMEbus Mailbox Address Compare Bit for VA15	state compare
ACR2	VMEbus Mailbox Address Compare Bit for VA14	state compare
ACR1	VMEbus Mailbox Address Compare Bit for VA13	state compare
ACR0	VMEbus Mailbox Address Compare Bit for VA12	state compare

The following AM-Codes are necessary for the mailbox access:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low

H = logical high

6.7.4 The VMEbus Requester

The CU824 offers a single level 2:1 pass requester with **(R)release (W)hen (D)one** or a four level **(R)release (O)n (R)equst** mode. The **RWD** requester releases the VMEbus mastership after the completion of each bus cycle and it has to request it for every following VMEbus cycle. The **ROR** method releases the VMEbus only, if the current VMEbus cycles have been completed and any other device in the VMEbus system requests for the busmastership. If there are no other requests, the **ROR** requester remains being busmaster even if it does not access the VMEbus.

The **RWDN** method is enabled within the **(B)oard (C)ontrol (R)egister** located at \$FE800013. If this bit is set to low, the release when done mode is active, otherwise the requester works in release on request mode. The contents of the BCR is cleared after reset and can be read back for verification.

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT
reset state	0	0	0	0	0	0	0	0
Release When Done	x	x	x	x	0	x	x	x
Release On Request	x	x	x	x	1	x	x	x

6.7.5 The VMEbus Arbiter

The CU824 contains a single level VMEbus requester for level 3. This allows the board to work as VMEbus controller as well as a bus slave in any combination.

The VMEbus arbiter function can be enabled, if jumper ARBE is installed. This link also enables all other system controller functions according to the following table.

VMEbus Signal	Slot 1 Function	Driver Type	not Slot 1 Function
System Clock	Output	Totem Pole	Tristate
System Reset	Input/Output	Open Drain	Input
Bus Error	Input/Output	Open Drain	Input
Bus Grant In 3	Input/Output	Totem Pole	Input



Please make sure, that only **one** system controller is enabled within a VMEbus system at a time, usually located in the leftmost slot. The use of more than one system controller will lead to improper operation and may cause permanent damage.

6.7.6 Preparations for VMEbus Multiprocessing

In case a VMEbus system should be configured for more than one VMEbus master, the user must verify, that only **one** system controller is enabled in the whole system. The system controller is usually located in the leftmost slot and drives the bus grant lines of slot 1. It supplies the system with the system clock, the system reset, and optionally the bus error and the bus clear information. All these lines, with the exception of the system reset and the bus error signal, are totem pole outputs and **must** be controlled **only** by the system controller within the VMEbus system. The system reset and the bus error lines are driven by open collector circuits and might be driven by more than one board.

6.7.7 VMEbus Timer

The **CU824** offers a bus monitor to supervise all VMEbus accesses. This time out counter terminates any cycle with the bus error signal, if the access exceeds a certain time, because a non existing device has been addressed or a defect device does not respond. The VMEbus BTO feature offers a time out sequence of 7 μ s starting at the falling edge of one or both VMEbus data strobes. It will be automatically activated, if the system controller function is enabled by jumper ARBE. If the board is not system controller, the bus monitor function of the VMEbus side is **not** disabled but the time out sequence is set to 120 μ s.

6.8 The PCI Interface Bus

The CU824 allows for a 32 bit PCI extension via its PCI interface bus connector. The connector contains all necessary signals and supply voltages for an external PCI device. In case the connected board uses the 3.3V supply, a current of 1A must not be exceeded. The 5V and +/-12V supply voltages are limited by the external supply of the CU824 and the connector pin current rating. The local PCI devices use the REQ0# and the GNT0# line to gain the busmastership of the PCI bus, i.e. they should not be used by other bus masters. The local PCI devices are fixed decoded and have no configuration area according to following address table.

Destination	from	to	Type	Size
VMEbus Std.Access	\$8000 0000	\$80FF FFFF	PCI-MEM	16Bit
SRAM Bank	\$8108 0000	\$810F FFFF	PCI-MEM	32Bit
DUART, Registers & IACK	\$FE80 0000	\$FEFF FFFF	PCI-I/O	8Bit/16Bit

The Pinout of the PCI interface connector:

Pin	Row a	Row b	Row c
1	VCC	VCC	VCC
2	AD0	AD1	AD2
3	AD3	GND	AD4
4	AD5	AD6	AD7
5	VDD	CBE0#	VDD
6	AD8	AD9	AD10
7	AD11	GND	AD12
8	AD13	AD14	AD15
9	PAR	CBE1#	SERR#
10	GND	n.c.	GND
11	STOP#	PERR#	LOCK#
12	TRDY#	IRDY#	DEVSEL#
13	FRAME#	CBE2#	n.c.
14	AD16	AD17	AD18
15	AD19	GND	AD20
16	AD21	AD22	AD23
17	VDD	CBE3#	VDD
18	AD24	AD25	AD26
19	AD27	GND	AD28
20	AD29	AD30	AD31
21	n.c.	GND	n.c.
22	REQ2#	RESET#	REQ0#
23	GNT0#	GND	GNT1#
24	GND	CLKB	GND
25	CLKD	GND	CLKA
26	GND	CLKC	GND
27	VDD	VCC	VDD
28	GNT3#	REQ1#	REQ3#
29	INTD#	INTC#	INTB#
30	n.c.	INTA#	n.c.
31	n.c.	n.c.	n.c.
32	+12V	GND	-12V

7. Register Overview

SAC @ \$FE800003	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ACR7	ACR6	ACR5	ACR4	ACR3	ACR2	ACR1	ACR0
compare function	VA23	VA22	STDE	SHTTE	VA15	VA14	VA13	VA12

VIE @ \$FE800007	D7	D6	D5	D4	D3	D2	D1	D0
read/write	VIER7	VIER6	VIER5	VIER4	VIER3	VIER2	VIER1	---

LIE @ \$FE80000B	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABIE	MBIE	SAIE	SBIE	P3IE	P2IE	P1IE	P0IE

SAA @ \$FE80000F	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	SAR0
source of PCI address	AD31	AD30	AD29	AD28	AD27	AD26	AD25	AD24

BCR @ \$FE800013	D7	D6	D5	D4	D3	D2	D1	D0
read/write	SMIE	RTIE	WDEN	RMCE	RWDN	FWP1	FWP0	FWPT

VIS @ \$FE800017	D7	D6	D5	D4	D3	D2	D1	D0
read only	VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	ARBE

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO

PIS @ \$FE80001F	D7	D6	D5	D4	D3	D2	D1	D0
read only	1	1	1	1	IRP3	IRP2	IRP1	IRP0

WDR @ \$FE800023	D7	D6	D5	D4	D3	D2	D1	D0
read/write	---	---	---	---	---	---	---	---

CMI @ \$FE800027	D7	D6	D5	D4	D3	D2	D1	D0
read/write	---	---	---	---	---	---	---	---

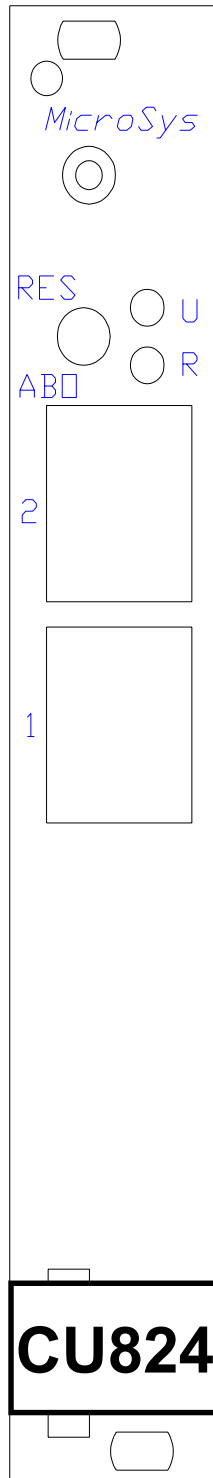
BRR @ \$FE80002B	D7	D6	D5	D4	D3	D2	D1	D0
read only	0	0	0	0	0	0	0	1

PLL @ \$FE80002F	D7	D6	D5	D4	D3	D2	D1	D0
read only	0	0	0	PLL0	PLL1	PLL2	PLL3	PLL4

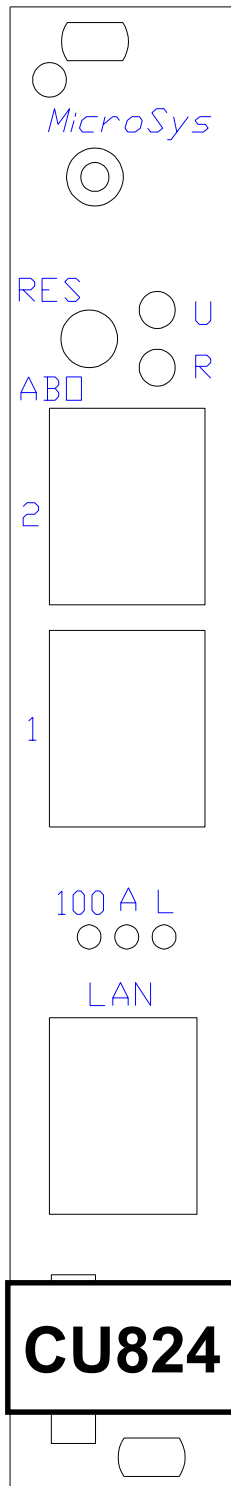
LCP @ \$FE800033	D7	D6	D5	D4	D3	D2	D1	D0
read/write	0	0	0	0	0	0	ULED2	ULED1

8. Front Panel Description

8.1 Front Panel Layout



8.2 Front Panel Layout with Network Option



8.3 Front Panel Connectors, LEDs & Switches

The front panel of the CU824 contains two RJ45 connectors used for the two serial I/O ports of the dual UART, a switch and two LEDs. Optionally, these two 8 pin RJ45 connectors can be replaced by two DSUB connectors. The switch has two functions. The center position is for normal operation, while the other positions generate a RESet or an ABOrt function.

With an optionally mounted ETH05, based on the Intel GD82559ER Ethernet controller, three additional LEDs and a RJ45 connector for 10/100Mbit twisted pair network are available at the front panel.



ting of ETH05 is not possible with DSUB option for serial I/O connectors.

8.3.1 Front Panel Connectors

Pin assignment of the DSUB / RJ45 serial connector 1 (ST3A/B) and 2 (ST4A/B)

Pin:	DSUB:	RJ45:
1	DCD	DSR
2	RXD	RTS
3	TXD	GND
4	DTR	TXD
5	GND	RXD
6	DSR	DCD
7	RTS	CTS
8	CTS	DTR
9	RI	---

Pin assignment of the optional RJ45 network connector LAN

Pin:	RJ45:
1	TX+
2	TX-
3	RX+
4	shield
5	shield
6	RX-
7	shield
8	shield

8.3.2 Front Panel LEDs

The USR and the RUN can be controlled by the user via the (L)ed (C)ontrol (P)ort at location \$FE800033. During a hardware reset all bits of this register are set to zero and both LEDs are switched on for a functional test. After the reset both LEDs are switched off. The two enable bits can be read back for verification.

LCP @ \$FE800033	D7	D6	D5	D4	D3	D2	D1	D0
reset state	0	0	0	0	0	0	0	0
user LED 1 on	0	0	0	0	0	0	X	1
user LED 1 off	0	0	0	0	0	0	X	0
user LED 2 on	0	0	0	0	0	0	1	X
user LED 2 off	0	0	0	0	0	0	0	X

The optional Ethernet piggyback ETH05 supports 3 additional LEDs.

100 This LED is switched on when connecting a 100Mbit Ethernet and is off with 10Mbit network attached.

A This LED is indicates Rx or Tx activity.

L Link integrity.

8.3.3 Front Panel Switches

The RESet switch position performs a local hardware reset to the CU824 and, in case the board is system controller, also a VMEbus system reset.

The ABOrt switch position generates a maskable interrupt to the MPC8240 on its IRQ0 line if the according bit within the (L)ocal (I)nterrupt (E)nable register at location \$FE80000F is set to high. The current status of the abort IRQ can be detected via the (L)ocal (I)nterrupt (S)tatus register at location \$FE80001F. The low active status of the abort IRQ is valid at any time, no matter if the enable bit is set or not.

Bit map of the (L)ocal (I)nterrupt (E)nable register:

LIE @ \$FE80000B	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABIE	MBIE	SAIE	SBIE	P3IE	P2IE	P1IE	P0IE
reset state	0	0	0	0	0	0	0	0
Abort Key & VMEbus ACFail enabled	1	x	x	x	x	x	x	x
Abort Key & VMEbus ACFail disabled	0	x	x	x	x	x	x	x

Bit map of the (L)ocal (I)nterrupt (S)tatus register:

LIS @ \$FE80001B	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	IRMB	SIO-A	SIO-B	SMON	RTC	ACF	WDGO
Abort Key IRQ active	0	x	x	x	x	x	x	x
Abort Key IRQ inactive	1	x	x	x	x	x	x	x

9. The ispLSI Programming Port

The programmable logic onboard the CU824 can be modified or updated via a PC controlled programming interface. The ISP programming port contains the necessary lines for serial programming of all ispLSI devices. Besides the programming option, also a JTAG mode is available for the ispLSI devices in hardware or emulation mode.

The pin assignment of the ISP port is shown in the following table:

Pin:	Signal:	Description:
1	SCLK/TCLK	serial clock in
2	GND	Ground
3	MODE/TMS	mode control in
4	n.c.	
5	ispEN	program enable
6	SDI/TDI	serial data in
7	SDO/TDO	serial data out
8	VDD	3,3 Volts

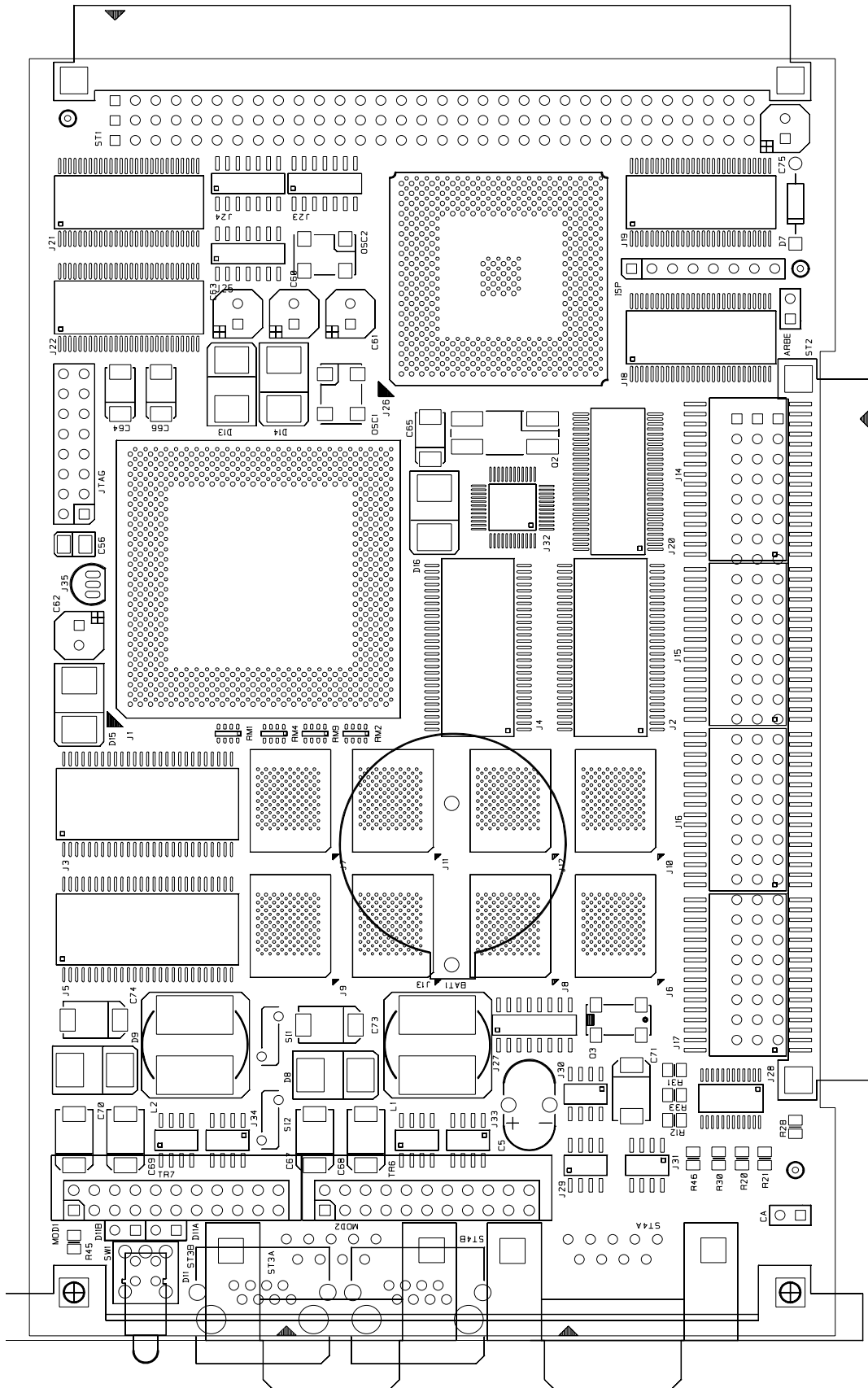
10. Summary of Jumper & Switches

Described function is valid, when jumper is set or link is intact !

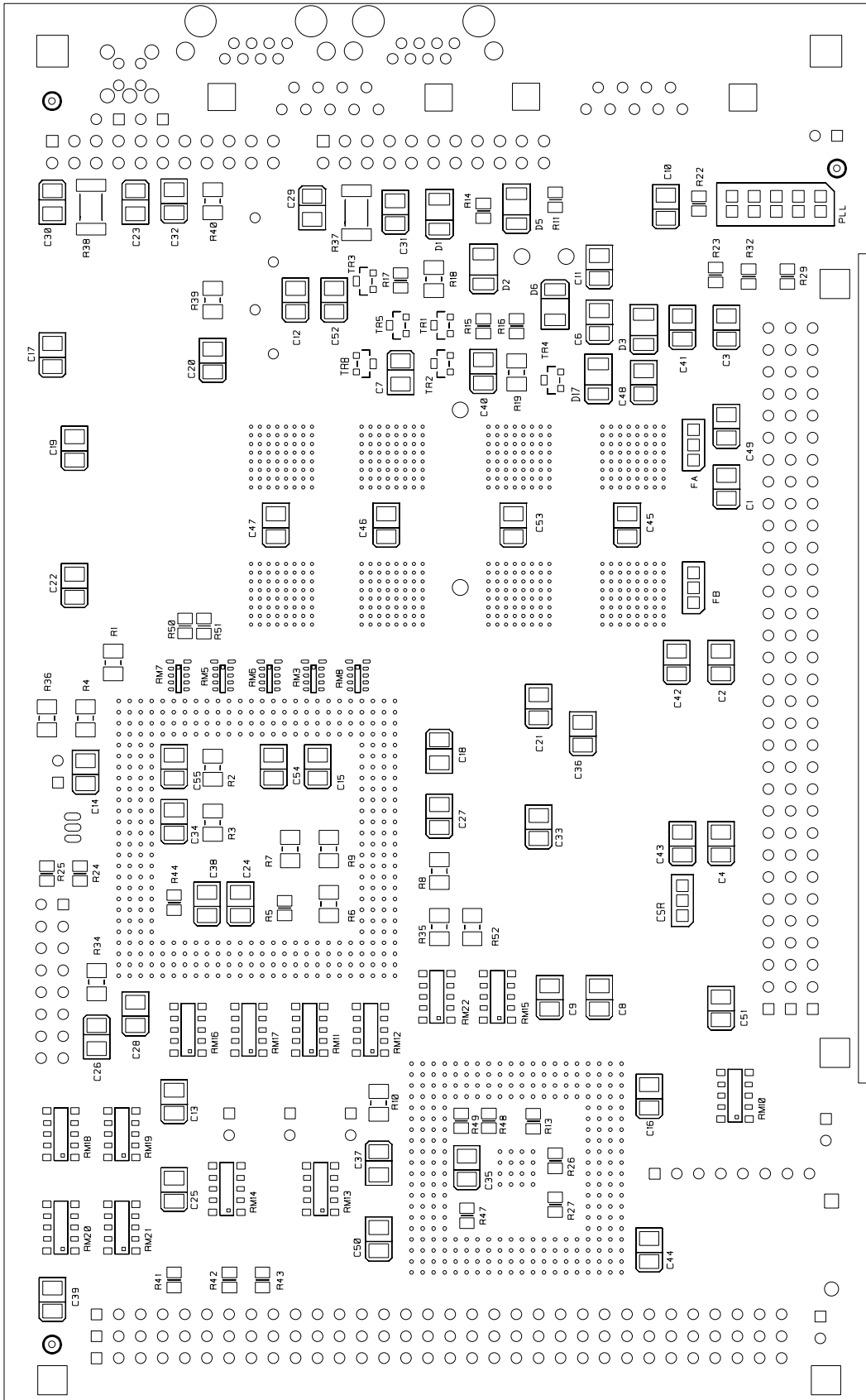
Size:	Name:	Default:	Position:	Function:
1x2	ARBE	#	1-2	System controller function enabled
			---	System controller function disabled
1x2	CA		1-2	Lithium battery connected
		#	---	Lithium battery disconnected
1x3	FA		1-2	Flash Bank A: ADV connected to RSC0
		#	2-3	Flash Bank A: ADV connected to GND
1x3	FB		1-2	Flash Bank B: ADV connected to RSC0
		#	2-3	Flash Bank B: ADV connected to GND
5x2	PLL	#	1-2	see chapter 6.5.4
		#	3-4	see chapter 6.5.4
		#	5-6	see chapter 6.5.4
		#	7-8	see chapter 6.5.4
		#	9-10	see chapter 6.5.4

Appendices

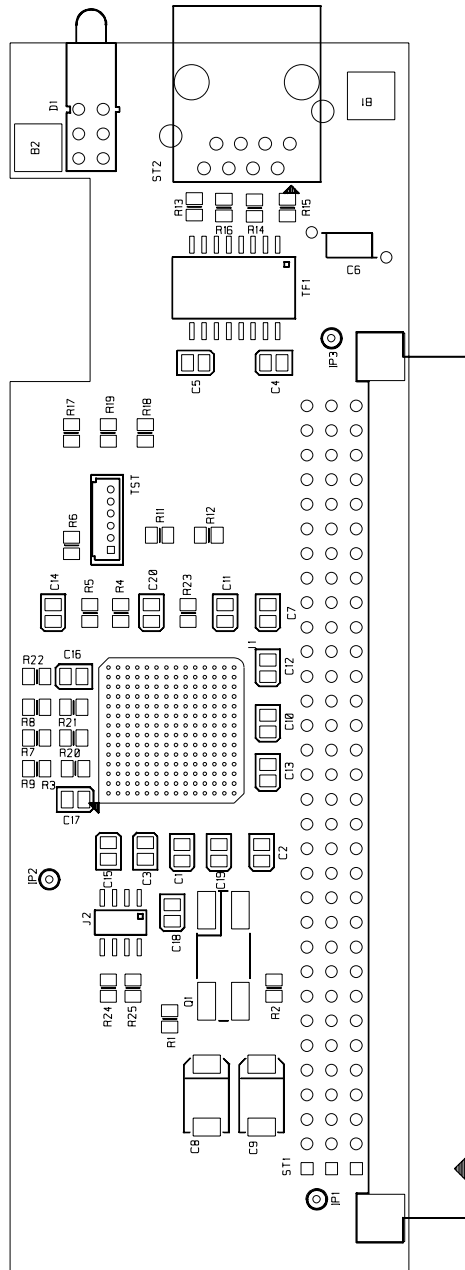
Appendix A: Layout Component Side CU824



Appendix B: Layout Solder Side CU824



Appendix C: Layout Component Side ETH05



Appendix D: Schematics CU824 (in printed Manuals only)

Appendix E: Schematics ETH05 (in printed Manuals only)